UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,781	02/18/2004	Ji-Yong Park	6161.0111.US	1632

58027 7590 04/20/2006

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,781	PARK ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-48* is/are pending in the application.

4a) Of the above claim(s) *2,5-7,9-12 and 14-46* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47 and 48* is/are rejected.

7)☒ Claim(s) *3,4,8 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/17/05, 3/7/06*. 3/16/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 2, 5-7, 9-12, and 14-46 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention/species, there being no allowable generic or linking claim. Election was made **without** traverse during the telephone conversation with Hae-Chan Park (Reg. #50,114) on June 21, 2005, and was confirmed in the reply filed 9/27/2005.

Claim Objections

Claims 3, 4, 18, 47, and 48 are objected to because of the following informalities:

Regarding claim 4, the limitation "A flat panel display device with polycrystalline silicon thin film transistor comprising:" is objected to. It is clear that there is more than one transistor in the display. Therefore, it is suggested the limitation be changed to "A flat panel display device with polycrystalline silicon thin film transistors ~~transistor~~ comprising:". Note claims 3, 8, 13, 47, and 48 have similar problems.

Further regarding claim 4, the claim defines "active channel regions of the thin film transistors". However, there is insufficient antecedent basis for "the thin film transistors" since the previous paragraph merely defines "a thin film transistor". It is suggested the limitation "a driving circuit portion comprising a thin film transistor" be changed to "a driving circuit portion comprising [[a]] thin film ~~transistor~~ transistors". It is also suggested the limitation "formed in an active channel region of the thin film transistors" be changed to "formed in each ~~an~~ active channel region of the thin film transistors". Further, there is insufficient antecedent basis for

"the one or more thin film transistors". Note that this claim has numerous inconsistencies in terms of how many transistors and channel regions are in both the pixel and driving sections. Considering Applicant is claiming an "average" number of grain boundaries, there must be more than one transistor in both the pixel and driving sections. The claim should be amended accordingly.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 47 and 48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 47, the limitations "an average number of grain boundaries of polycrystalline silicon which are formed in an active channel region of the driving thin film transistor" and "an average number of grain boundaries of polycrystalline silicon which are formed in an active channel region of the switching thin film transistor" render the claim indefinite. It is unclear how a single channel region can have an average number of grain boundaries. In order to have an average, there must be more than one. Note that claim 48 has the same problem.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 48 is rejected under 35 U.S.C. 102(b) as being anticipated by Zhang et al. (US Pat. 5,614,733, hereinafter Zhang).

Regarding claim 48, Figure 3 of Zhang discloses a flat panel display device (liquid crystal display) (col. 1, lines 49-51) comprising: a pixel portion 3 divided by gate lines and data lines (not labeled) and equipped with a thin film transistor (TFT) (col. 1, lines 53-60) driven by signals applied by the gate lines and data lines; and driving circuit portion 2 comprising a TFT (col. 1, lines 53-60) connected to the gate lines and data lines respectively to apply signals to the pixel portion. It is inherent that the average number of grain boundaries in the channel regions of the driving TFTs that meet a current direction line is more than zero, since does not disclose a crystallization method that would result in grain boundaries being exactly parallel with the current line direction. Furthermore, Zhang discloses a method of crystallizing the amorphous semiconductor film used to make the active (channel) region of the driving and pixel TFTs, wherein the crystallinity of portions used to make the channels of driving TFTs is greater than the crystallinity of the portions used to make the channel of the pixel TFTs, thereby enhancing the carrier mobility of the driving TFTs (col. 4, lines 35-40 and col. 8, lines 54-62). Therefore, it is inherent that the average number of grain boundaries in the driving TFTs that meet a current

direction line is at least one less than the average number grain boundaries in the pixel TFT that meet a current direction line.

Claim 48 is rejected under 35 U.S.C. 102(b) as being anticipated by Miyanaga et al. (US Pat. 5,705,829, hereinafter Miyanaga).

Regarding claim 48, Figures 1 and 5F of Miyanaga discloses a flat panel display device (liquid crystal display) comprising: a pixel portion divided by gate lines and data lines and equipped with a thin film transistor (TFT) (Figure 5F) driven by signals applied by the gate lines and data lines; and a driving circuit portion comprising one or more TFTs (Figure 5F) connected to the gate lines and data lines respectively to apply signals to the pixel portion, wherein the one or more thin film transistors at the driving circuit portion include an average number of grain boundaries of polycrystalline silicon which are formed in active channel regions that meet a current direction line is more than zero and at least one or more less than the average number of grain boundaries of polycrystalline silicon which are formed in active channel regions of the TFT installed at the pixel portion and meet a current direction line for a unit area of active channels. Note that Miyanaga discloses the grain boundaries in the channel of the driving (peripheral) TFT grew in a direction *approximately* parallel with the current direction (col. 2, lines 30-34) and that the grain boundaries in the channel of the pixel (switching) TFT grew in a direction approximately perpendicular to the current direction (col. 2, lines 34-50 and col. 8, lines 42-51). Since the crystal grains in the driving TFT are not perfectly parallel to the current direction (which would be impossible due to the somewhat random nature of crystal growth), it is inherent that at least some grain boundaries meet the current direction line. Therefore, it is inherent that

the average number of grain boundaries that meet the current direction in the driving TFTs is more than zero, but at least one less than that of the pixel TFTs.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroshima et al. (US PGPub 2004/0079944, hereinafter Hiroshima) in view of Zhang.

Regarding claim 47, Figure 8 of Hiroshima discloses an organic electroluminescent device comprising switching TFTs and driving TFTs (paragraph [0068]). Hiroshima does not disclose the specific limitations regarding the average number of grain boundaries in the channel regions of the switching and driving TFTs. Figure 3 of Zhang discloses a flat panel display device (liquid crystal display) (col. 1, lines 49-51) comprising: a pixel portion 3 divided by gate lines and data lines (not labeled) and equipped with a thin film transistor (TFT) (col. 1, lines 53-60) driven by signals applied by the gate lines and data lines; and driving circuit portion 2 comprising a TFT (col. 1, lines 53-60) connected to the gate lines and data lines respectively to apply signals to the pixel portion. As stated above, Zhang inherently discloses the average number of grain boundaries in the driving TFTs that meet a current direction line is at least one less than the average number grain boundaries in the pixel TFT that meet a current direction line.

In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Hiroshima by including the TFT structures of Zhang for the purpose of obtaining low leakage current pixel TFTs and a high current mobility driving TFTs (col. 4, lines 35-40).

Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroshima in view of Miyanaga.

Regarding claim 47, Figure 8 of Hiroshima discloses an organic electroluminescent device comprising switching TFTs and driving TFTs (paragraph [0068]). Hiroshima does not disclose the specific limitations regarding the average number of grain boundaries in the channel regions of the switching and driving TFTs. Figures 1 and 5F of Miyanaga discloses a flat panel display device (liquid crystal display) comprising: a switching TFT for transmitting data signals; and a driving TFT for driving the display device so that a certain amount of current flows through the device according to the data signals, wherein an average number of grain boundaries of polycrystalline silicon which are formed in active channel regions of the driving TFT and meet a current direction line is more than zero and at least one or more less than the average number of grain boundaries of polycrystalline silicon which are formed in active channel regions of the switching TFT and meet a current direction line for a unit area of active channels (see above rejection of claim 48). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Hiroshima by including the TFT structures taught by Miyanaga. The ordinary artisan would have been

motivated to modify Hiroshima in the manner described above for the purpose of obtain an organic electroluminescent display wherein the OFF current of the switching TFT is minimized and the current mobility in the driving TFT is increased (col. 8, lines 42-53).

Allowable Subject Matter

Claims 3, 4, 8, and 13 would be allowable if rewritten or amended to overcome the claim objections, set forth in this Office action.

The reasons for allowance were provided in the Office Action mailed on November 7, 2005.

Response to Arguments

Applicant's arguments filed February 7, 2006 have been fully considered but they are not persuasive.

Applicant argues, "the Examiner has made it clear that the Examiner interprets Miyanaga as teaching that the number of grain boundaries that meet the current direction in the driving TFTs is zero. Therefore, Miyanaga does not teach each and every element as set forth in claim 48". After further review of the Miyanaga reference, it was found that Miyanaga teaches "TFTs constituting a peripheral circuit are formed with a crystalline silicon film in which crystals grew in a direction *approximately* parallel with a direction along which carriers of the TFTs flow..." (emphasis added) (col. 2, lines 30-34). In light of this teaching, the Examiner has changed the interpretation to more accurately reflect the teachings of Miyanaga. As stated above, since the

grain boundaries are not perfectly parallel to the current direction line, there must be at least some grain boundaries that intersect the current direction line. Therefore, the average number of grain boundaries that meet the current direction line must be greater than zero.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

April 15, 2006